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DESIGN AND ANALYSIS OF SINGLE LAYER QUANTUM DOT-CELLULAR AUTOMATA BASED 1-BIT COMPARATORS

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Abstract

Quantum dot-cellular automata (QCA) technology has emerged as a promising avenue for designing nanometer-scale computational circuits. In digital logic circuits, comparators serve as fundamental components for comparing binary values. This paper introduces and implements two 1-bit QCA-based comparator designs. These proposed QCA implementations are compact, utilizing only a single layer and exhibiting reduced complexity compared to previously reported designs. Functional validation of the proposed QCA structures has been conducted using the QCA Designer tool. Simulation results of the proposed comparators demonstrate significant improvements over existing counterparts in terms of the number of QCA cells, area requirements, cost, and complexity efficiency. Moreover, the proposed structures exhibit extremely low energy consumption. Therefore, these QCA-based comparators present viable options for low-power digital applications.

Keywords: 1-bit comparator, Low power, QCA technology, Single QCA layer

1. Introduction

The relentless pursuit of higher performance and increased integration in microelectronics, driven by Complementary Metal Oxide Semiconductor (CMOS) scaling, has been a cornerstone of technological advancement for decades [1]. However, the continued densification of transistors on a chip has led to escalating power dissipation within digital systems. Moreover, the constraints imposed by physical limitations on parameters such as effective channel length and gate oxide thickness have prompted a quest for alternative materials and device structures to sustain scaling efforts [1]-[4].

Quantum Dot-Cellular Automata (QCA) technology has emerged as a promising candidate to circumvent the challenges facing traditional CMOS technology. Offering advantages like rapid switching speeds, enhanced packing densities, and reduced energy consumption, QCA presents an enticing avenue for future device scaling [3], [5]. In QCA, logical states are encoded based on the position of electrons within quantum dots, with data transmission facilitated by electrostatic interactions among adjacent cells, in contrast to conventional CMOS where current flow conveys information [4].

Building logical circuits on the nanoscale with QCA entails employing various strategies for data transmission and computation [4], [7]. However, due to the reliance on electrostatic repulsions for data propagation, ensuring reliable information flow necessitates the incorporation of clocking mechanisms

in QCA circuit designs [8]. These clocking mechanisms orchestrate four sequential phases—switch, hold, release, and relax—driving the movement of electrons within QCA cells [9], [10].

Basic building blocks in QCA, such as the inverter and majority gate, enable the implementation of diverse logical functions, with operations like AND and OR achieved through manipulation of input logic states [4], [8], [11]. To enhance design flexibility, coplanar and multilayer crossover techniques are employed for wiring crossovers. While coplanar crossovers use a single layer and distinct cell orientations to avoid interference, multilayer crossovers leverage multiple layers to minimize area overhead, albeit with increased manufacturing complexity [4], [7].

In recent years, extensive research has proposed various computational and storage circuits based on Quantum-dot Cellular Automata (QCA), including Arithmetic and Logic Units (ALU), counters, multipliers, nano-sensor data processors, adders, and subtractors. This diversity of QCA-based logic and memory structures positions QCA technology as a crucial contender for future computing systems. Among these structures, the comparator plays a critical role in numerous digital applications, such as processors, microcontrollers, and digital communication systems. It facilitates the comparison of two n-bit numbers, provided either serially or in parallel, and determines three possible outcomes: equality, inequality (greater than), or inequality (less than).

Several studies have explored QCA implementations of single-bit comparators using various gate configurations. For instance, one study introduced a single-bit comparator utilizing reversible Feynman QCA gates, comprising 87 cells and occupying an area of 0.11 μm2. Another investigation proposed two 1-bit comparator implementations using layered-T AND and OR gates, requiring 40 and 37 QCA cells, respectively, with occupational areas of 0.032 μm2 and 0.028 μm2. Additionally, a 1-bit comparator employing a universal gate was proposed, utilizing 58 QCA cells with an area of 0.055 μm2 and a latency of 3 clock cycles.

Other approaches include a multilayer QCA-based comparator employing a five-input majority gate, resulting in a 1-bit comparator with a delay of three clock cycles. Despite these efforts, significant improvements in the number of QCA cells and area requirements have remained elusive. Furthermore, recent studies have introduced XNOR gate-based implementations of multi-bit comparators, aiming for reliable and efficient structures. A coplanar 1-bit QCA comparator structure was also developed, leveraging fundamental QCA logic gates and achieving reduced cell count, occupied area, latency, and cost compared to previous designs. Moreover, a recent proposal presents a 1-bit QCA comparator utilizing a single layer and 31 QCA cells, occupying an area of 0.04 μm2, along with two AND gates, one OR gate, and three inverters.

Given the considerable interest in high-performance, area- and energy-efficient comparator circuits, this paper focuses on designing and implementing area-efficient comparator structures based on QCA technology. The functionality of the proposed circuits is evaluated using a specialized QCA design tool, and comprehensive comparisons are made with recently published designs. The evaluation results demonstrate significant reductions in cell count and area requirements compared to the best-performing existing designs.

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The remainder of this paper is structured as follows: Section 2 introduces the proposed 1-bit comparator structures. Section 3 explores the functional validity, performance evaluation, energy dissipation estimation, and comparison with recently reported designs. Finally, conclusions are drawn in Section 4.

2. PROPOSED COMPARATOR STRUCTURES

This section introduces two area-efficient 1-bit comparator designs based on QCA technology. Figures 1 and 2 depict the proposed single-layer 1-bit comparators. The comparator circuit compares two binary inputs labeled A and B, generating three output signals: FA=B, FA>B, and FA<B, according to the logic functionality detailed in Table 1. The algebraic expressions describing the behavior of the 1-bit comparator are provided in Equation (1).

$FA{=}B{=}A^{-}\oplus B^{-} FA{=}B{=}A\oplus B\ FA{>}B{=}A{\cdot}B^{-} FA{>}B{=}A{\cdot}B\ FA{<}B{=}A^{-}{\cdot}B FA{<}B{=}A{\cdot}B$

Table 1. One-bit comparator truth table

A	B	FA=B	FA>B	FA<B
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

The first proposed single-layer 1-bit comparator (Design A) is illustrated in Figure 1. This structure utilizes three clock zones to influence data flow direction and propagate computational results to output cells. It includes two 3-input majority gates to obtain outputs FA>B and FA<B, with FA=B generated by feeding FA>B and FA<B to an additional majority gate. Design A employs only 23 cells without any wiring crossovers. Notably, outputs FA>B and FA<B are achieved using clock zones 0 and 1, while FA=B is produced using clock zones 0, 1, and 2. The second proposed 1-bit single-layer comparator circuit (Design B) is depicted in Figure 2. Compact and requiring only 14 QCA cells with an area of 0.02 μm2, this design eliminates the need for crossovers. Outputs FA<B, FA>B, and FA=B are obtained using clock zones 0 and 1. Design B demonstrates a 64.3% reduction in cell count compared to Design A and features lower output delay, clocked using two clock zones.

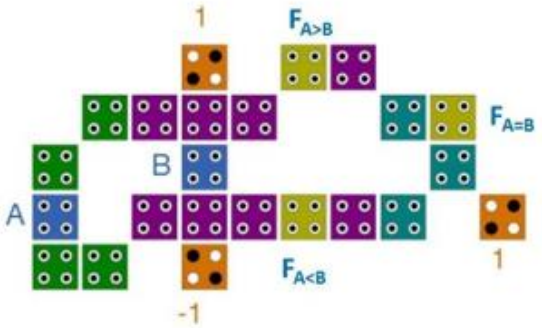

Figure 1. The first proposed structure - Design A

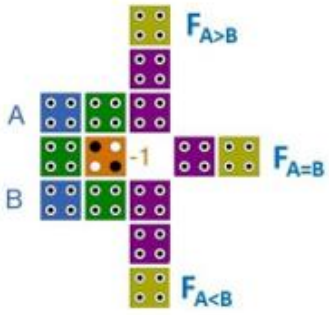

Figure 2. The second proposed structure - Design B

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3. RESULTS AND DISCUSSIONS

The QCADesigner-ver-2.0.3 simulation tool [32] was utilized to assess the functionality of the proposed 1-bit comparator structures and determine their structural costs, including the number of cells, area, and output delay. Simulation parameters were configured as outlined in Table 2.

Figure 3 illustrates the simulation results of the first proposed structure (Design A). These results confirm the functional validity of the proposed design, aligning with the logical values specified in Table 1. Notably, when input A equals input B, only the corresponding output (FA=B) is activated. Conversely, if input A is greater than input B, only output FA>B is asserted, and when input A is lower than input B, output FA<B is activated. Additionally, outputs FA>B and FA<B exhibit a delay of 0.5 clock cycles from the inputs, while output FA=B experiences a delay of 0.75 clock cycles.

Table 2. Simulation configuration

Parameter	Value
QCA cell width	18 nm
Cell height	18 nm
Diameter of the quantum dot	5 nm
Number of samples	12800
Number of iterations per sample	10000
Radius of effect	65 nm
Layer separation	11.5 nm

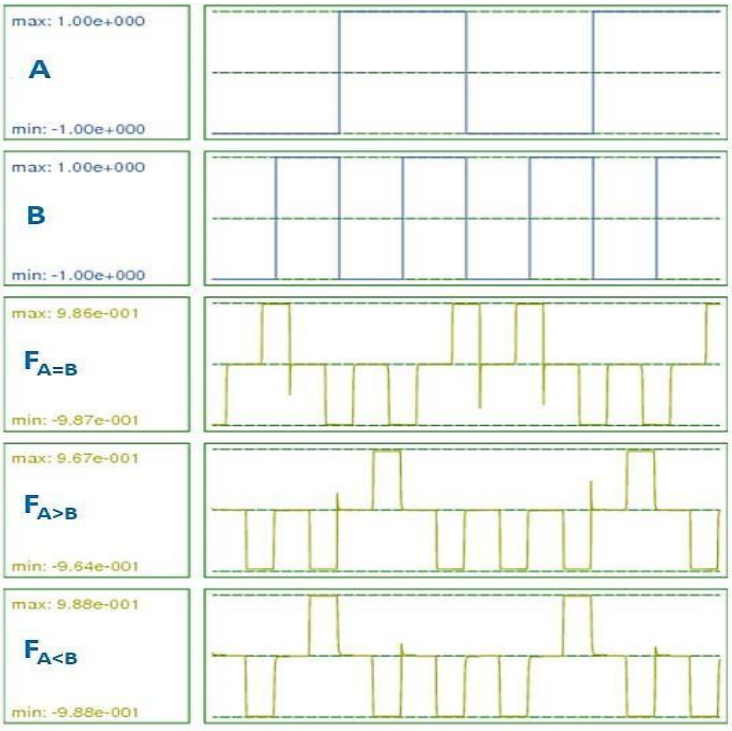

Figure 3. Simulation results of the first proposed 1-bit comparator-Design A

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The simulation results for the second proposed 1-bit comparator (Design B) are depicted in Figure 4. Evidently, the proposed design successfully achieves the intended comparison functionality. Moreover, all outputs in this structure are obtained with a delay of 0.5 clock cycle after the application of input signals. Consequently, the second proposed structure operates 33% faster than its first counterpart.

Furthermore, Figure 5 provides a comparison of the proposed structures in terms of cell count (structural complexity) and occupational area. As observed, the second proposed structure (Design B) notably reduces the number of QCA cells and occupational area requirements compared to Design A. Specifically, the achieved reductions in cell count and occupational area are 39% and 33%, respectively.

Additionally, the QCA Designer-E tool [33] was employed to compute the energy dissipation of the proposed structures. Figure 6 illustrates the total and average energy dissipations of the proposed designs. Notably, both proposed designs exhibit low total and average energy dissipation levels. In comparison to the first proposed design (Design A), the second proposed design (Design B) demonstrates lower total and average energy dissipation values. The improvements in total and average energy dissipations are found to be 30.5% and 30.55%, respectively.

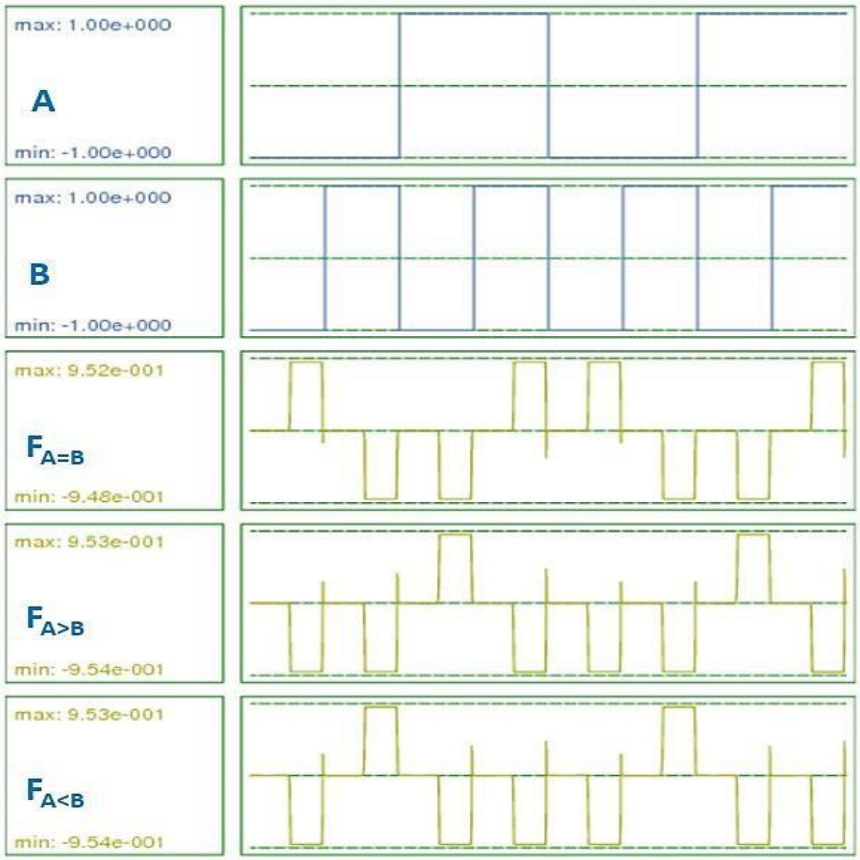

Figure 4. Simulation results of the second proposed 1-bit comparator-Design B

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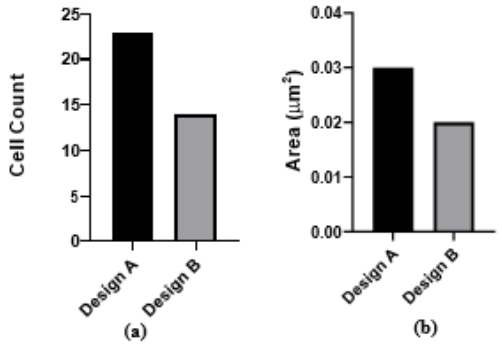

Figure 5. Comparisons of (a) cell count and (b) area of the proposed comparator structures

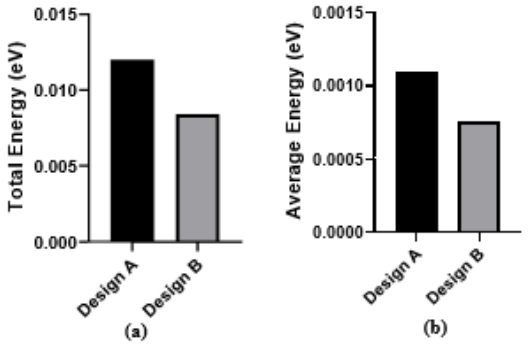

Figure 6. Comparisons of (a) total energy and (b) average energy dissipations of the proposed comparator structures

Additionally, key comparison factors in designing and evaluating QCA-based structures are cost and efficient complexity factors. Indeed, the cost value is contingent upon the area of the QCA structure in μm2 and the output delay per clock cycle, as expressed in Equation (2) [31], [34]:

Cost=Area×Delay2 (2)Cost=Area×Delay2 (2)

On the other hand, the efficient complexity (EC) is determined using the formula provided in Equation (3) [30]:

Efficient Complexity=Cell count×Area1/n (3)Efficient Complexity=Cell count×Area1/n (3)

where nn is the number of QCA layers.

Figure 7 illustrates a comparison of the proposed designs in terms of cost and efficient complexity values. As depicted, the second proposed design (Design B) exhibits lower cost and efficient complexity values compared to its first counterpart. The achieved reductions in both values have reached approximately 70%.

Table 3 summarizes and compares the proposed structures with other existing QCA-based comparators.

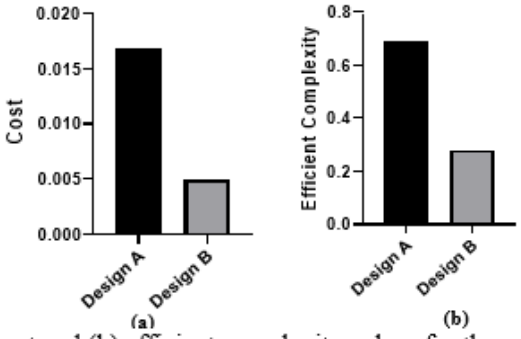

Figure 7. Comparisons of (a) cost and (b) efficient complexity values for the proposed comparator structures

Table 3. Comparisons between the proposed comparators and recent designs

The comparison parameters include cell count, area, delay, crossover type, cost, and efficient complexity (EC) values. Both proposed 1-bit comparator structures (Design A and B) outperform recently reported designs. Specifically, they achieve a reduction of 25.8% and 54.5%, respectively, in the number of required cells compared to the most recent structure proposed in [26]. Additionally, the proposed QCA-based structures occupy less area compared to the best reported design [26]. The reduction in efficient complexity (EC) value reaches up to 26% relative to [26].

Furthermore, while the area occupied by the first proposed structure (Design A) is smaller than that presented in [25], this reduction is primarily due to increased QCA layers rather than logic design, resulting in a higher EC value. Conversely, the structure proposed in [31] has a similar occupational area to Design A, but it relies on coplanar crossover, which may pose reliability issues during manufacturing.

Notably, the second proposed design (Design B) surpasses all recent reported designs in terms of cell count and area requirements, achieving reductions of up to 54.5% and 75%, respectively, compared to the most recent comparator design in [26]. The cost and efficient complexity (EC) values are also reduced by 78% and 77.4%, respectively, relative to [26].

In conclusion, the proposed structures offer alternative 1-bit QCA-based comparator designs with efficient occupational area and cell count, eliminating the need for multilayer and coplanar crossover wiring techniques.

4. CONCLUSION

This article introduced and thoroughly evaluated two different 1-bit comparator QCA-based structures. The logical correctness of the proposed comparators was verified using the QCA Designer tool, and energy dissipation values were estimated using the QCA Designer-E tool. Performance comparisons with previously reported designs, considering key design factors such as area, cell count, delay, cost, and efficient complexity values, were included. Both proposed 1-bit comparator structures (Design A and B) achieved significant reductions in cell requirements compared to the most recent comparator design, as well as substantial improvements in efficient complexity. In future, these QCA designs can be expanded to n-bit comparators for the efficient construction of arithmetic circuits.

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