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DESIGN OF QUANTUM VOLTAGE COMPARATOR BASED CMOS SUCCESSIVE APPROXIMATION ANALOG TO DIGITAL CONVERTER

J.Joshua Daniel Raj, Dr. Sam Harison, Dr. Karthikeyan

Department of Electrical and Electronics Engineering,
New horizon college of Engineering, Bangalore

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ABSTRACT
A novel Design of Quantum Voltage (QV) Comparator based CMOS Successive Approximation Analog to Digital Converter (ADC) is been implemented. The Successive Approximation ADC utilizes sequentially staged QV Comparator with Successive Approximation Register (SAR) and Voltage Scaling DAC circuit. For a 3-bit ADC, the design consumes 14.6 nA of current, 0.101 pW of power at a conversion speed of 0.25 MHz with INL and DNL of 0.2 LSB and 0.3 LSB respectively. This design represents a drastic improvement in power consumption with higher precision compared to previously reported ADC implementations. The simulation results show that the QV comparator based SAR ADC is preferable for the next-generation deep sub-micron low voltage CMOS ADC. An experimental prototype was simulated at 0.34 µm CMOS with a supply voltage of 5 V using Cadence Analog Design Environment and Magic Layout Editor.
Keywords: QV Comparator, Successive Approximation ADC, DAC

I. INTRODUCTION

Digital signal processing has proliferated because of its flexibility, reproducibility, reliability and programmability. With the rapid evolution in modern semiconductor technology, digital signal processing systems have a lower overall cost compared to analog systems [1] [2]. In many areas analog circuits are replaced by their digital counterparts such as wireless communication and digital audio. But as the interface between the real physical world and virtual digital world, A/D and D/A converters are always required.

Analog-to-digital converters (ADCs) are key design blocks in modern microelectronic digital communication systems. With the fast advancement of CMOS fabrication technology, more and more signalprocessing functions are implemented in the digital domain for a lower cost, lower power consumption, higher yield, and higher reconfigurability. This has recently generated a great demand for low-power, low-voltage ADCs that can be realized in a mainstream deep-submicron CMOS technology.

Specifications of these converters emphasize high dynamic range and low spurious spectral performance. Another hurdle to achieve full system integration stems from the power efficiency of the A/D interface circuits supplied by a low voltage dictated by the gate-oxide reliability of the deeply scaled digital CMOS devices. It has been

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observed recently that these interface analog/mixed-signal circuits are gobbling a larger chunk of the chip area as well as total power consumption; hence it becomes essential to accomplish an optimized design from both the architecture and the circuit standpoints. To achieve high linearity, high dynamic range, and high sampling speed simultaneously under low supply voltages in
deep submicron CMOS technology with low power consumption has thus far been conceived of as extremely challenging.

II. ADC ARCHITECTURES

At present, there exists a variety of ADCs with different architectures, resolutions, sampling rates, power consumptions, and temperature ranges. These ADCs are used in different applications - from mobile communication devices to measure equipment - according to the characteristics of ADCs. Since the performance - sampling rate, resolution, and power consumption - of an ADC is basically determined by its architecture, one single ADC type cannot cover all applications. For instance, flash (parallel) ADCs can be used in high speed and low resolution applications. Because of its parallel architecture, all conversions are done in one cycle with many comparators. On the other hand, a successive approximation ADC can be used in lowspeed and high-resolution applications since the conversions are done in many cycles with only one comparator. Therefore, it is important to properly choose an ADC for each particular application.

Among the variety of ADC architectures, there are four most popular ADC architectures presently used. These are as follows:

Flash: The flash ADC operates at very high speed with lower resolution. It is also called a parallel ADC due to its parallel operation.

Pipelined: The pipelined ADC can operate at a high speed, but it is slower than the flash. It covers a wide range of applications because of its flexible resolution and speed.

Successive approximation register (SAR): The SAR ADC is suitable for low power and medium-to-high resolution applications with medium speed. Sigma-delta (∑Δ): The ∑Δ ADCs are used for high resolution and low speed applications.

Figure 1 shows the tradeoff between resolutions and sampling rates of the above popular ADC architectures. The application ranges for each architecture are also shown.

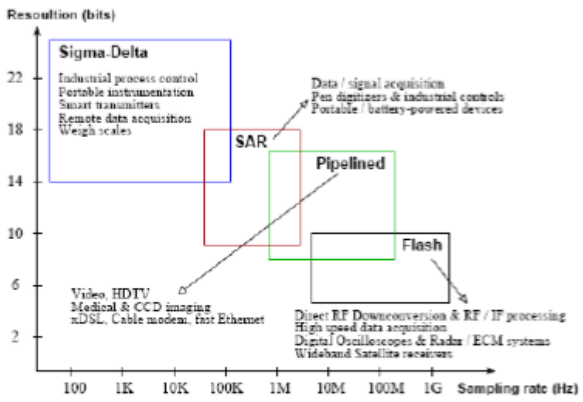

Fig. 1. Tradeoff between resolutions and sampling rates

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III. SUCCESSIVE APPROXIMATION ADC ARCHITECTURE

The successive approximation register (SAR) - commonly called successive approximation converter - is widely used in industrial control applications and battery powered applications because of its good balance between speed and power consumption. Figure 2 illustrates the architecture of the SAR ADC that consists of one comparator, a DAC, and a successive approximation register. The conversion algorithm is similar to the binary search algorithm. First, the reference voltage, Vref,
provided by DAC is set to the $VFSR/2$
to obtain the MSB. After getting the MSB, the

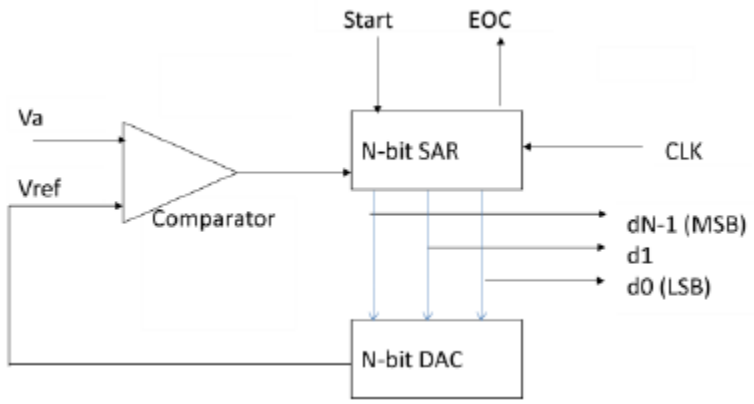

Fig. 2. Block diagram of a successive approximation (SAR) ADC

SAR moves to the next bit with $VFSR/4$
or
3/4 VFSR depending on the result of the MSB. If the MSB is "1", then$Vref$ = 3/4 $VFSR$, otherwise$Vref$ = $VFSR/4$. This sequence will continue until the LSB is obtained. Figure 3 shows how the reference voltages are implemented in a 3-bit SAR ADC.

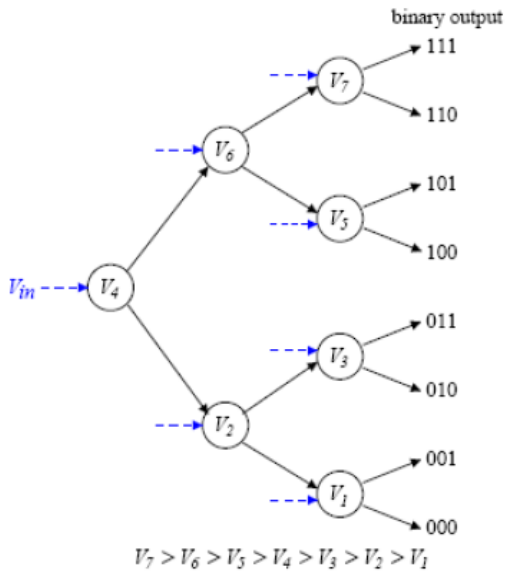

Fig. 3. Reference voltage tree in a 3-bit SAR ADC

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Note that V7 is the largest reference voltage, and V1 is the smallest reference voltage. To get a binary output, 3 comparisons are needed, while 7 comparisons are needed in the flash architecture. For a 10-bit resolution, the SAR only needs 10 comparisons with a single comparator, but the flash ADC needs 1023 comparisons with 1023 comparators. There are large savings in power consumption, but the SAR ADC needs n cycles for n-bit resolution, while the flash ADC and the pipeline ADC need 1 cycle and m (number of stages) cycles, respectively. Therefore, this SAR architecture is very attractive for low power applications with a medium sampling rate.

IV. QV SUCCESSIVE APPROXIMATION ADC

The ADC using the proposed QV comparator is a full SAR type. As shown in figure 4, the ADC consists of three blocks: Comparator, Successive Approximation Registers and a voltage scaling DAC. An analog input voltage Va, is connected to QV Comparator. The Va is compared with the reference voltage Vref from the DAC circuit. The SAR implemented is a simple Serial in Parallel out (SIPO) Shift Register with a Clock. The digital output is provided by the output of the registers namely d0, d1and d2, d0 being the LSB and d2 the MSB.

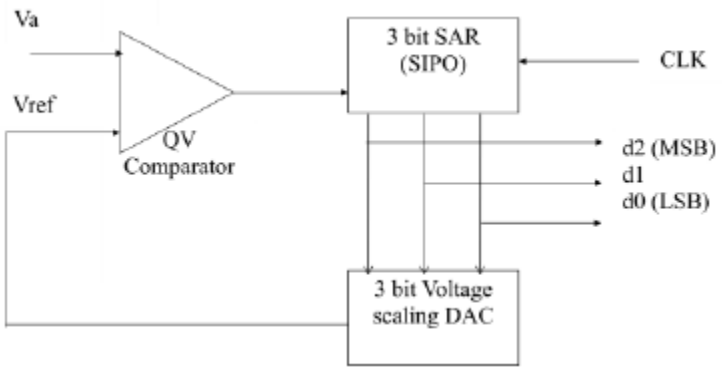

Fig. 4. Block diagram of modified QV successive approximation (SAR) ADC

V. QUANTUM VOLTAGE COMPARATOR

The new QV comparator has been devised from the simple transconductance amplifier [3] with the application of the TIQ comparator concept to generate the internal reference voltages. It is a type of differential voltage comparator. Since this comparator has two inputs for analog signals, the common mode noise rejection is much better. This is the reason why most conventional ADCs use differential comparators.

A. Simple Transconductance Amplifier

A simple transconductance amplifier (STA) circuit consists of two circuits, a current mirror and a differential pair. Figure 5 shows the schematic diagram of the current mirror and the differential pair. The current mirror is devised to provide a constant cur rent at both drains of transistor Q1 and Q2 in Figure 5(a). As the gate of Q1 is connected to its drain, the transistor Q1 is always in saturation mode. Therefore, the current I2 is fixed at a constant current that is equal to the current I1. In the differential pair shown in Figure 5(b), the difference between voltage V3 and V4

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determines the current I3 and I4, where I3+I4 = Ib. Transistor Qb is a current source, which produces a fixed current that depends on the voltage Vb.

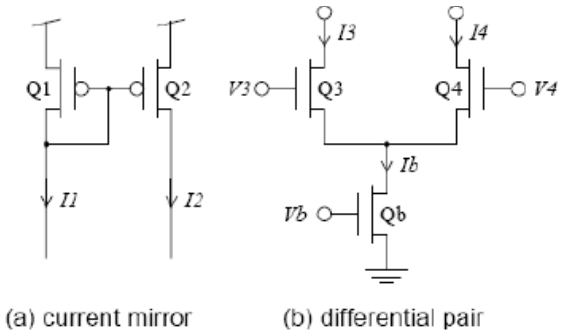

Fig. 5. Schematic of the current mirror and the differential pair [3]

By combining the current mirror (at the top) and the differential pair (at the bottom), we can devise the STA circuit. This is commonly used as a transconductance amplifier that generates a current output depending on the difference between two input voltages. This circuit can also be used as a voltage amplifier by taking a voltage at the output instead of a current. Many ADCs use this voltage amplifier as a comparator to compare a reference voltage with an input voltage. The simple voltage amplifier has been used in the proposed QV comparator.

B. The QV Comparator

The schematic diagram of the proposed QV comparator is shown in Figure 6(a). One can see there is no difference from the STA schematic diagram except for changes in the W/L ratios. The VTC of the STA is similar to the VTC of the inverter. Figure 6(b) shows the VTC of the QV comparator. The C0 and C2 curves show the voltage output of one QV comparator and the voltage output of two cascading QV comparators, respectively. Both the logic zero values of the C0 and C2 curves are not close to ground because of the lower limitation of the voltage out called the "Vmin problem" in [3]. One can see different low voltage limits in each curve of Figure 6(b). This low voltage limit problem can be solved by adding a gain booster. The gain booster in the ADC architecture makes the comparator output transition sharp and also produces a full rail-to-rail swing. In Figure 6(b), there are three different curves, C1, C2, and C3, simulated by cascading two QV comparators. These curves illustrate that how different reference voltages are internally obtained. In conventional differential comparators, the transistor sizes are standardized and the input Va is taken from a Vref generated by a resistor ladder circuit. Therefore, all 2n − 1 comparators for an n-bit flash ADC are identical, but the externally supplied reference voltages are different. On the other hand, the proposed QV comparator has different transistor sizes for transistors Q3 and Q4, while transistor Q1 and Q2 are

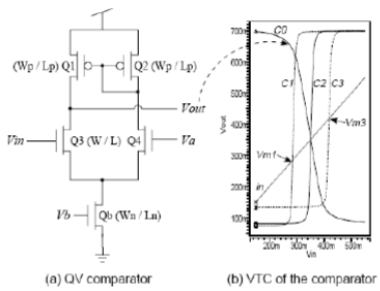

Fig. 6. Schematic of the QV comparator and its voltage transfer characteristic [4]

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identical. In addition, the input voltage Va and the bias voltage Vb are fixed at a constant voltage between GND and VDD. With this intentional mismatch in the differential pair, the reference voltages can be internally supplied to the comparators. The curve C2 in Figure 6(a) has been obtained for the case of equal sizes of the differential pair. If transistor Q3 is larger than Q4, the C1 and Vm1 will be obtained as the VTC and the Vref, respectively. Conversely, if transistor Q4 size is larger than Q3, the C3 and Vm3 will be obtained as the VTC and the Vref, respectively.

VI. VOLTAGE SCALING DAC CIRCUIT

Voltage Scaling DAC converts the reference voltage, Vref, to a set of 2N voltages that are decoded to single analog output by the input digital word. The decoder network simply connects one of the V1, V2, …, V2N voltages to Vout. Voltage scaling normally
uses series resistors connected between VREF and ground to selectively obtain these limits. For an N-bit converter, the resistor string would have at least 2N segments. These segments can all be equal or the end segments may be partial values, depending on the requirements. The resistor strings has been replaced using NMOS transistors in depletion mode. The value of output voltage is calculated using formulae such as

$$vout = \frac{vref}{8}(n - 0.5) = \frac{vref}{16}(2n - 1)$$

The value of resistances can be varied in a transistor placed in a depletion mode using sizing. We have taken marginally a sizing factor of 3 4 / or a width of 0.18µm in all the transistors that is being implemented in the design, so each transistor in the DAC is having different scaling sizes in order to provide varied resistance string. The implemented DAC is shown in figure 7.

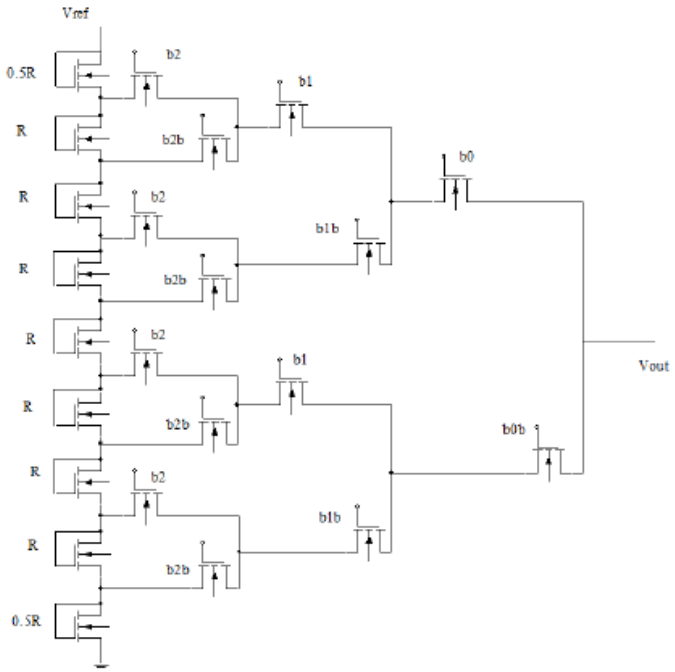

Fig. 7. Voltage Scaling DAC using transistor string (sizing used 0.7, 0.6, 0.5, 0.4, 0.3, 0.2, 0.15, 0.1, 0.05)

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VII. EXPERIMENTAL RESULTS

The experimental results of the QV SAR ADC are discussed in this section. The ADC has been designed using the Cadence Analog Design Environment and the Layout in Magic layout Editor tool.
The output of the QV Comparator is in figure 8. It shows that logic zero is not exactly "0 Volts", called the Vmin problem.

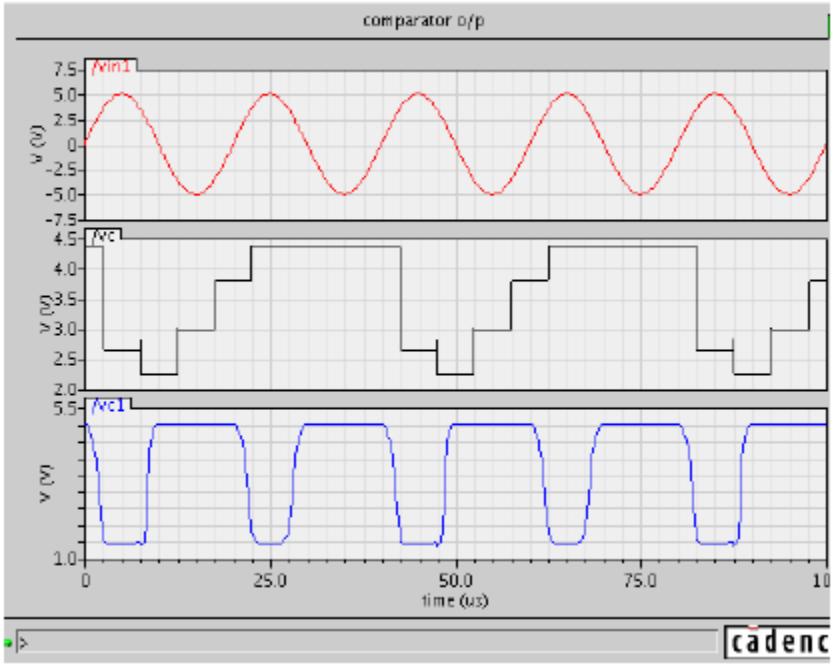

Fig. 8. QV comparator output; Vin1 is the analog input, Vc is the output of the DAC and Vc1 is the output of the QV Comparator

The output of the DAC is shown in figure 9. Voltage scaling normally uses series resistors connected between Vref and ground to selectively obtain these limits. For an N-bit converter, the resistor string would have at least 2N segments. These segments can all be equal or the end segments may be partial values, depending on the requirements. The resistor strings has been replaced using NMOS transistors in depletion mode. The output of the DAC verifies that it is monotonic. The switches almost eliminate the glitches which occur during the switching activity of the change in the successive bits during conversion.

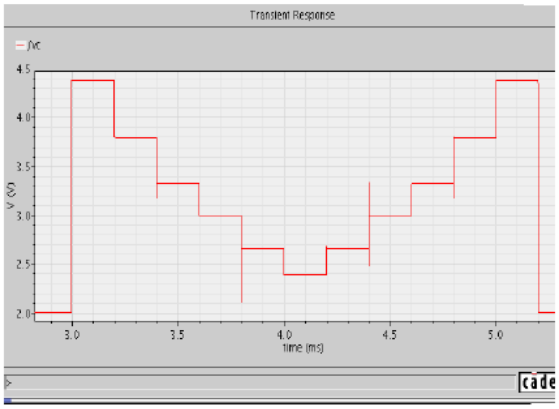

Fig. 9. Output of the 3-bit Voltage Scaling DAC

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The analog input sine wave (with a 10 Vp-p) and the corresponding digital output of the QV SAR ADC is shown in figure 10. The conversion speed is found to be 0.25 MHz. The INL and DNL error is found to be 0.2 LSB and 0.3 LSB respectively.

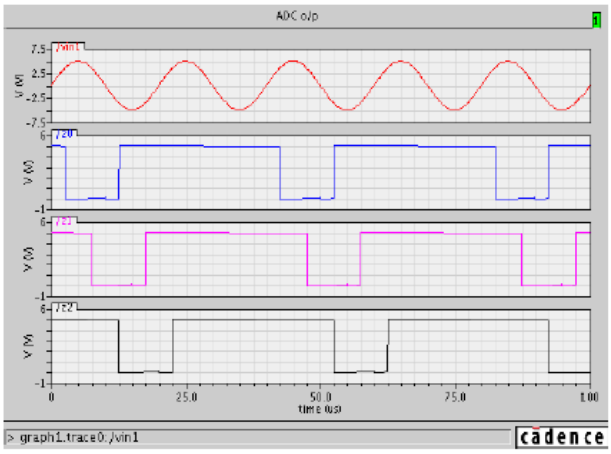

Fig. 10. Input Output Characteristics of QV SAR ADC circuit

The Layout for the design is done using the Magic Layout Editor Tool and it is simulated in HSpice simulator. The input and output characteristics as obtained by the simulator are shown in figure 11.

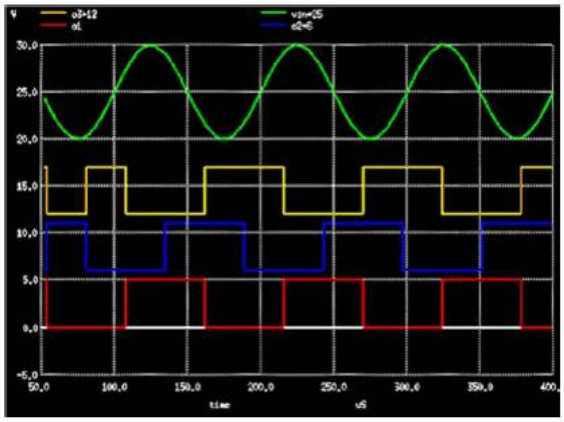

Fig. 11. Simulation of the Layout with HSpice Simulator

The instantaneous power dissipation is plotted in figure 12. The instantaneous power dissipation increases for every clock cycle. The clock is used in the shift register in the design. The average power dissipated by the QV SAR ADC is 0.101 pW.

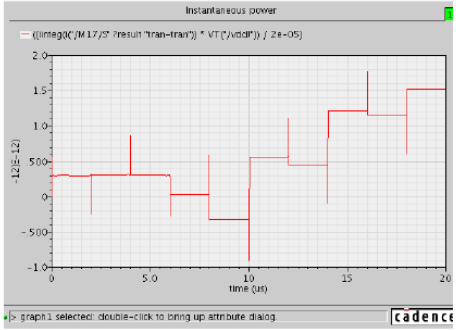

Fig. 12. Instantaneous power dissipation characteristics

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VIII. ELECTRICAL SPECIFICATIONS

Parameter	QV SAR ADC
Resolution	3 bit
Conversion Rate	0.25 MHz
INL	0.2 LSB
DNL	0.3 LSB
Technology	0.34 µm TSMC
Power Dissipation	0.101 pW
Supply Voltage	5 V
Supply Current	14.6 nA

Table 1: Electrical Specifications

Parameter QV SAR ADC Resolution 3 bit Conversion Rate 0.25 MHz INL 0.2 LSB DNL 0.3 LSB Technology 0.34 µm TSMC Power Dissipation 0.101 pW Supply Voltage 5 V Supply Current 14.6 nA

The electrical specifications of the designed Successive Approximation ADC using QV Comparator are listed in the Table 1.

IX. CONCLUSION

To reduce noise problems in the ADCs, a new differential comparator, called the quantum voltage (QV) comparator, was designed for SAR ADC. The simulation results show that the QV comparator is preferable for the next generation deep submicron low voltage CMOS ADC.

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