Jupiter Publications Consortium

Vol. 1(4), pp. 172-177, 4, MAR, 2016
ISSN Print : 2454-1435 © 2015 IJRMMAE
ISSN Online : 2454-1443 © 2015 IJRMMAE
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International Journal of Research in Mechanical, Mechatronics and Automobile Engineering

High Speed CMOS Comparator

Dr.M.Roberts Masillamani
Department of Computer Science and Engineering,Shadan College of Engineering and Technology HYD,T.S,INDIA

Received 10, February 2016 | Accepted 04, March 2016

Abstract

Analog-to-Digital conversion method is an digital procedure in which an analog sign is changed, except altering its quintessential contents, into a digital signal. Latched comparators use positive remarks mechanism (aids in the input signal) to re-generates (amplifies) the analog input sign into a Full-scale digital stage output signal .This paper presents a CMOS comparator that reduces the common propagation prolong and hence gives greater speed. The proposed design is simulated in 0.25µm CMOS Technology by means of using Tanner EDA Tools. CMOS Comparator shows that the universal propagation extends of the comparator, TPD, is 1.7872e-9 seconds, with a 1.0 V supply voltage.

Keywords: Comparator, CMOS, Dynamic Latched Comparator.

Introduction

Cmos entirely dynamic latched comparators are majorly used in Analog to Digital converters (ADCs), statistics receivers and Memory Sense Amplifiers (SAs) because they grant high speed, decreased energy consumption, full swing output and high enter impedance[2]. Dynamic latched comparators hire re-generative stage, which consist of cross coupled inverters, to provide a effective remarks mechanism. This regenerative stage is used to convert a differential voltage, from the input stage, into a full swing digital output country at a very quick price [8].

Literature assessment and objectives

D. Y. Kim et. al. [3] "The Design of the High Speed Amplifier Circuit for Using in the Analog Subsystems" a excessive velocity cmos based totally an amplifier circuit and this amplifier circuit is further used to design a high pace cmos comparator, which is further utilized in specific analog to digital converters. The designed amplifier and comparator circuit is connected in complementary trend to grant the reap stage to make bigger speed.

Daniel Schinkel et. al. [6] investigated "A Double-Tail Latch-Type Voltage Sense Amplifier" a latch type voltage sense amplifier that has one tail transistor which limits the total modern-day flowing via the both of the output branches; it shows sturdy dependency on pace and offset voltage with one-of-a-kind common-mode input voltage Vcom. To alleviate this disadvantage, the comparator with separated input-gain stage and output-latch stage was introduced. This separation made this comparator have a lower and extra steady offset voltage over huge input common-mode voltage (Vcom) degrees and function at a decrease provide voltage (VDD) as well.

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Heung Jun Jeon et. al. [3] investigated "A CMOS low-power low-offset and high-speed utterly dynamic latched comparator" that a novel dynamic latched comparator has lower offset voltage and greater load drivability than the traditional dynamic latched comparators. With two additional inverters inserted between the input- and output-stage of the conventional double-tail dynamic comparator, the achieve previous the regenerative latch stage is improved. The complementary version of the regenerative latch stage, which presents larger output force contemporary than the traditional one at a confined area, is implemented.

Existing CMOS Comparator

Figure1 shows the double tail totally dynamic comparator is designed in CMOS Technology the use of Tanner EDA Tools. It consists of an input stage accompanied by using a regenerative latch stage and an output buffer stage. Comparator utilizes two tail transistors, one transistor is used for input stage and 2nd tail transistor is used for latching or re-generative stage. The comparator can be used for lesser operating voltages.

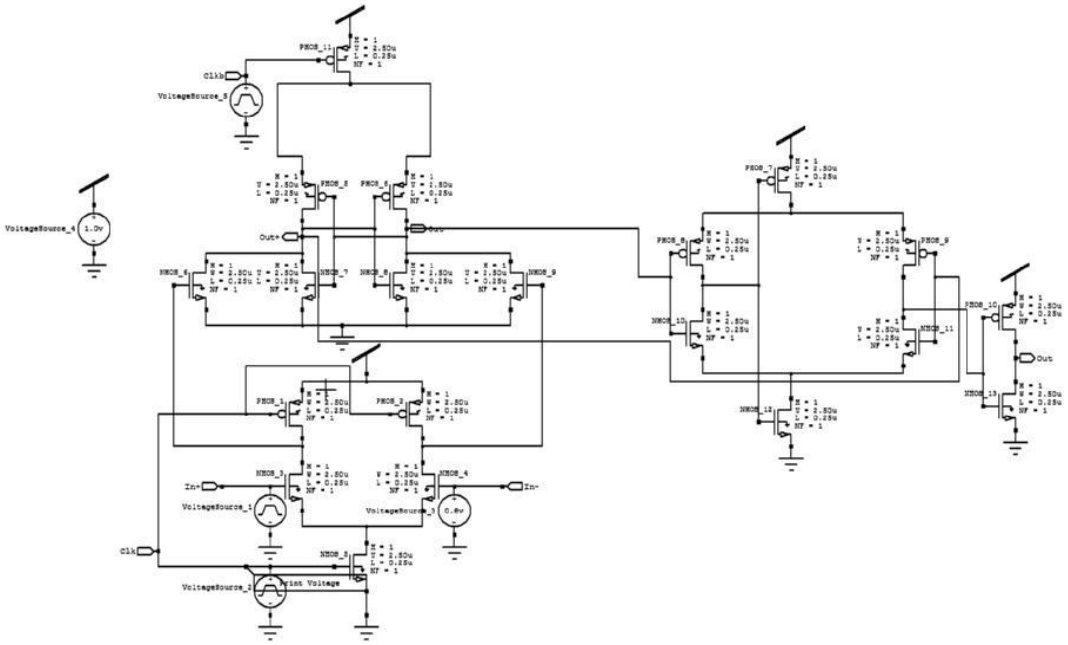

Figure 2: Dual Tail fully dynamic CMOS comparator[6].

The double tail comparator offers a giant contemporary in the re-generative stage for speedy re-generation and permits much less modern in the input differential stage to decrease offset. During the reset section when Clk =0, nmos transistor NMOS_5 is off or in cut-off mode, nmos transistors NMOS_3 and NMOS_4 are off whereas pmos transistors PMOS_1 and PMOS_2 are on, these pmos transistors will charge the drains of PMOS_1 and PMOS_2 transistor toward VDD . And due to this fact NMOS_6 and NMOS_9 will purpose the output nodes out+ and out- to discharge towards floor on account that Clkb =1 so pmos transistor PMOS_11 will be in cut-off mode.

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During the re-generation segment when Clk =VDD the tail transistors NMOS_5 and PMOS_11 will flip on and the voltages at the drain terminals of PMOS_1 and PMOS_2 drops down. NMOS transistors NMOS_3 and NMOS_4 are on while pmos transistors PMOS_1 and PMOS_2 are off. The transistors NMOS_6 and NMOS_9 are then used to ignore the differential voltage from the input nodes to the re-generating stage. The cross joined inverters begin to re-generate the differential voltage as NMOS_6 and NMOS_9 can't clamp the outputs to ground. The plan is simulated the use of 0.25µm CMOS Technology the usage of Tanner EDA Tools, with a 1.0 V supply.

Design Process of this Work

A high speed latched comparator the use of positive remarks based again to back latch stage, appropriate for pipelined Analog to Digital converter, with decreased prolong and high pace is proposed

During the RESET PHASE, when Clk is LOW (Clk =0), transistor NMOS_3 is in off nation and pmos transistors PMOS_3, PMOS_9, PMOS_4, PMOS_10 are in on state. Transistors NMOS_1 and NMOS_2 are in cutoff mode. Switch transistors PMOS_3, PMOS_9, PMOS_4, and PMOS_10 will cost the drains of transistors NMOS_ 1 and NMOS_2 and the output nodes Outp and Outn towardsVDD .

In the REGENERATION PHASE, when Clk is HIGH (Clk =1),

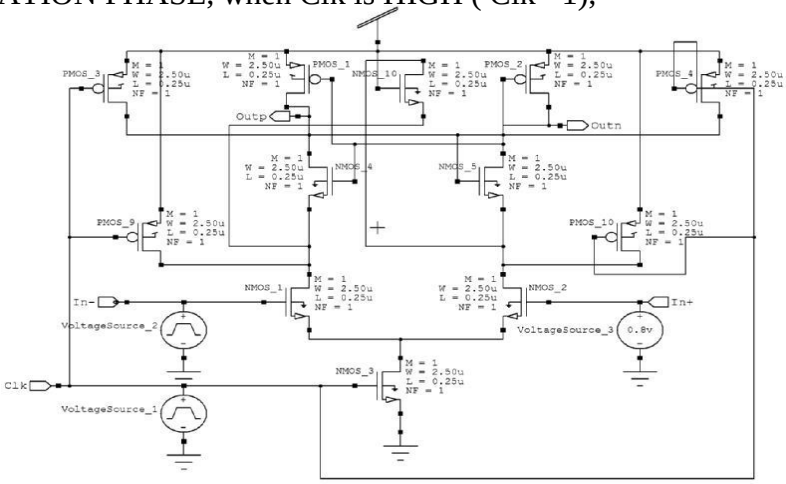

Figure 3: High speed CMOS comparator.

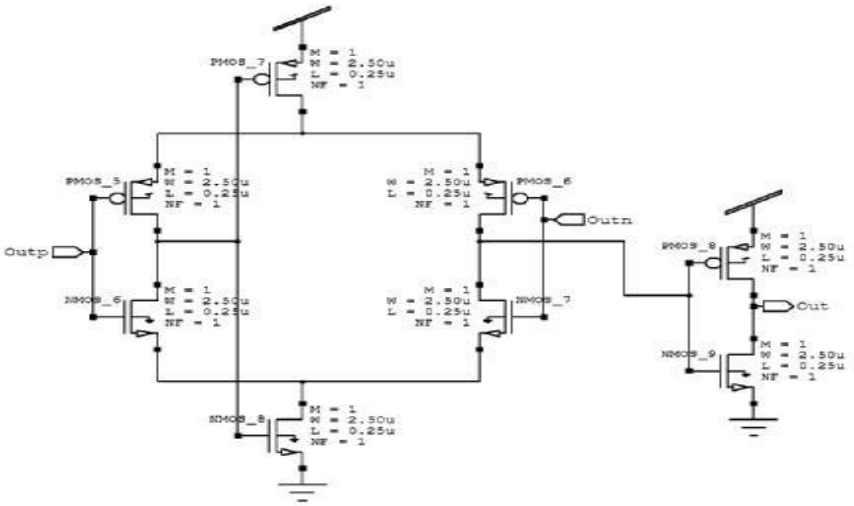

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Figure 4: High speed CMOS comparator Output Stage.

The system begins by way of turning the transistor NMOS_3 on and straight away an modern 'I' starts to drift and the drain of transistor NMOS_3 starts offevolved to discharge toward ground (Gnd).

In this succession the differential enter transistors NMOS_1 and NMOS_2 are became on. The currents of transistors NMOS_1 and NMOS_2, (at the drain terminal) will begin to pull the output nodes Outp and Outn in the direction of Gnd. Due to the distinction of voltages between the enter signals, the cutting-edge at the drain terminals of transistors NMOS_ 1 and NMOS_2 will be different.

Now in the regeneration mode the output node are discharging in the direction of Gnd and pmos transistors PMOS_1 and PMOS_2 will come in saturation mode as the voltage at output nodes falls under VDD |Vtp |. So a robust effective comments will decorate the output signal. This regeneration manner is accomplished when one Nmos transistor comes in cutoff mode.

The sketch is simulated the usage of 0.25µm CMOS Technology the use of Tanner EDA Tools. Proposed plan well-knownshows decreased extend and excessive pace with a 1.0 V supply. This layout can be used where excessive speed and low propagation delay are the foremost parameters.

Simulation

The sketch is simulated in the design is replicated in 0.25µm CMOS Technology using Tanner EDA Tools. Comparator design indicates decreased delay and excessive speed with a 1.0 V supply. Finally simulation consequences of the comparator are given below, when a differential sign is utilized as an input to the latched comparator. The simulated results are proven below:

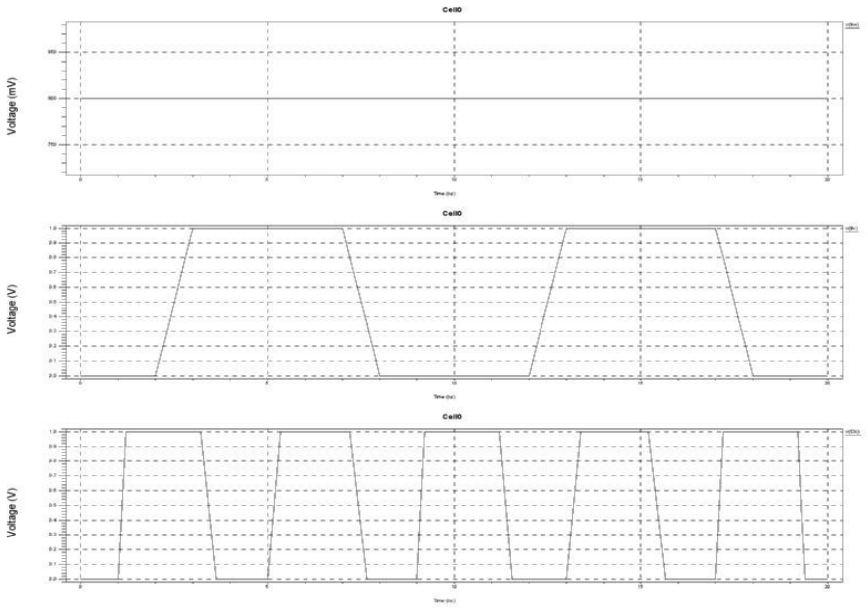

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Fig. 5: Simulation Results - waveform 1 and waveform 2 shows the analog input applied to the comparator, waveform 3 shows the clock signal applied.

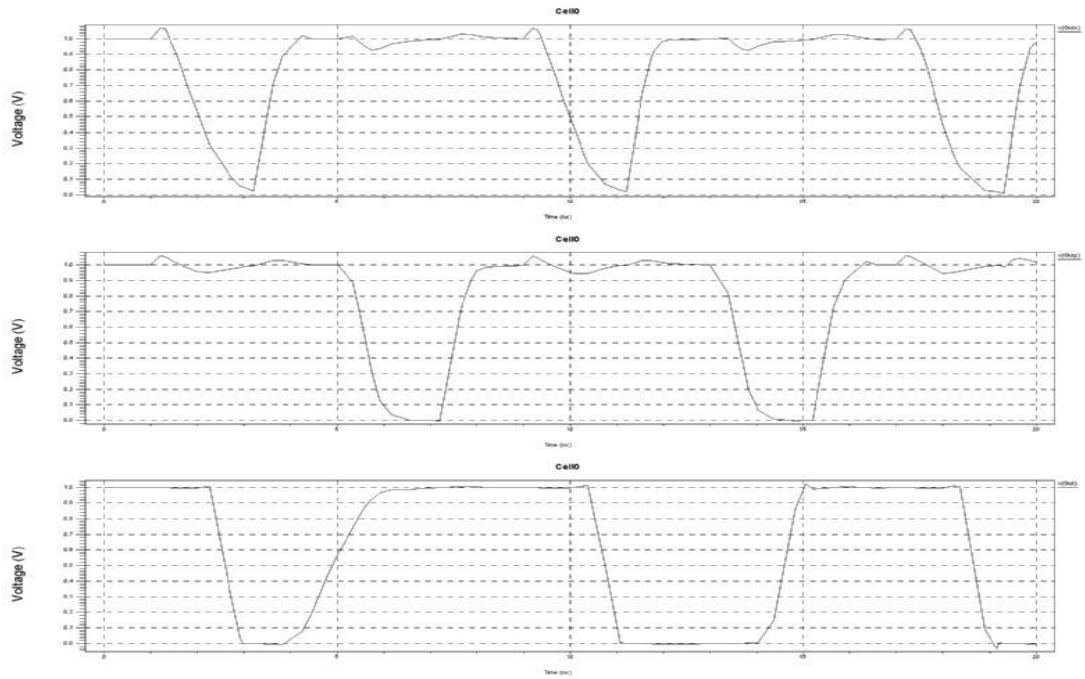

Fig. 6: Simulation Results (waveform 1 shows the output at node Outn, waveform 2 shows the output at node Outp, waveform 3 shows the output at node Out).

Results and Future Scope

The shorter propagation delay, the greater the pace of the circuit and vice-versa. Delay time is measured at 90% transition of the point. The propagation delay is decided using two primary time intervals, which is TPHL and TPLH. TPLH is the delay time measured when output is changing from good judgment zero to common sense 1 and TPHL is from logic 1 to 0.The overall propagation prolong of the above circuit (Fig three and Fig 4) comes out to be 1.7872e-009 seconds.

Table 1: Results Obtained.

Comparators	**Existing Comparator**	**This Work**
Parameters	A	B
Total Propagation Delay	5.954 ns	1.787ns

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The Total Propagation Delay of the proposed comparator comes out to be 1.7872ns which is less than lengthen of Comparator A having a extend of 5.954 ns. So the Proposed Comparator shows decreased lengthen and for this reason it will show higher speed as in contrast to the comparators mentioned in [4].

In the future one can minimize the enter referred latch offset voltage, energy consumption, Hysteresis response.

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